

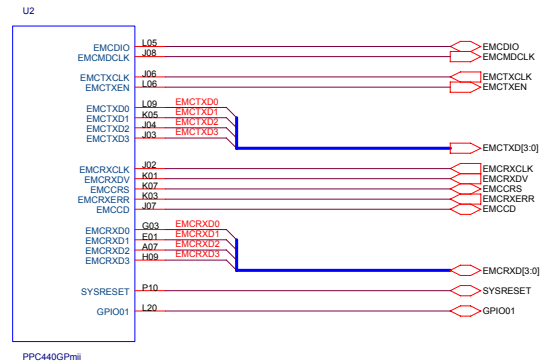
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## IBM Power PC

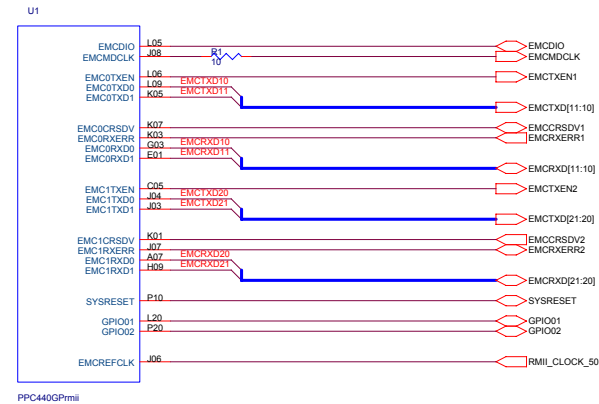
Note: For Reference Only

### 440GP Embedded Processor

NOTE: For either single MII device or dual RMII devices, but not both.



MII Connections

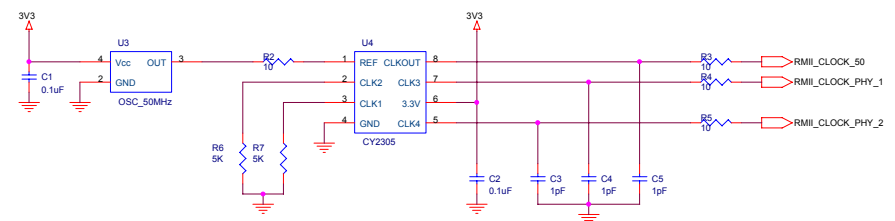


RMII Connections

#### Revision Updated:

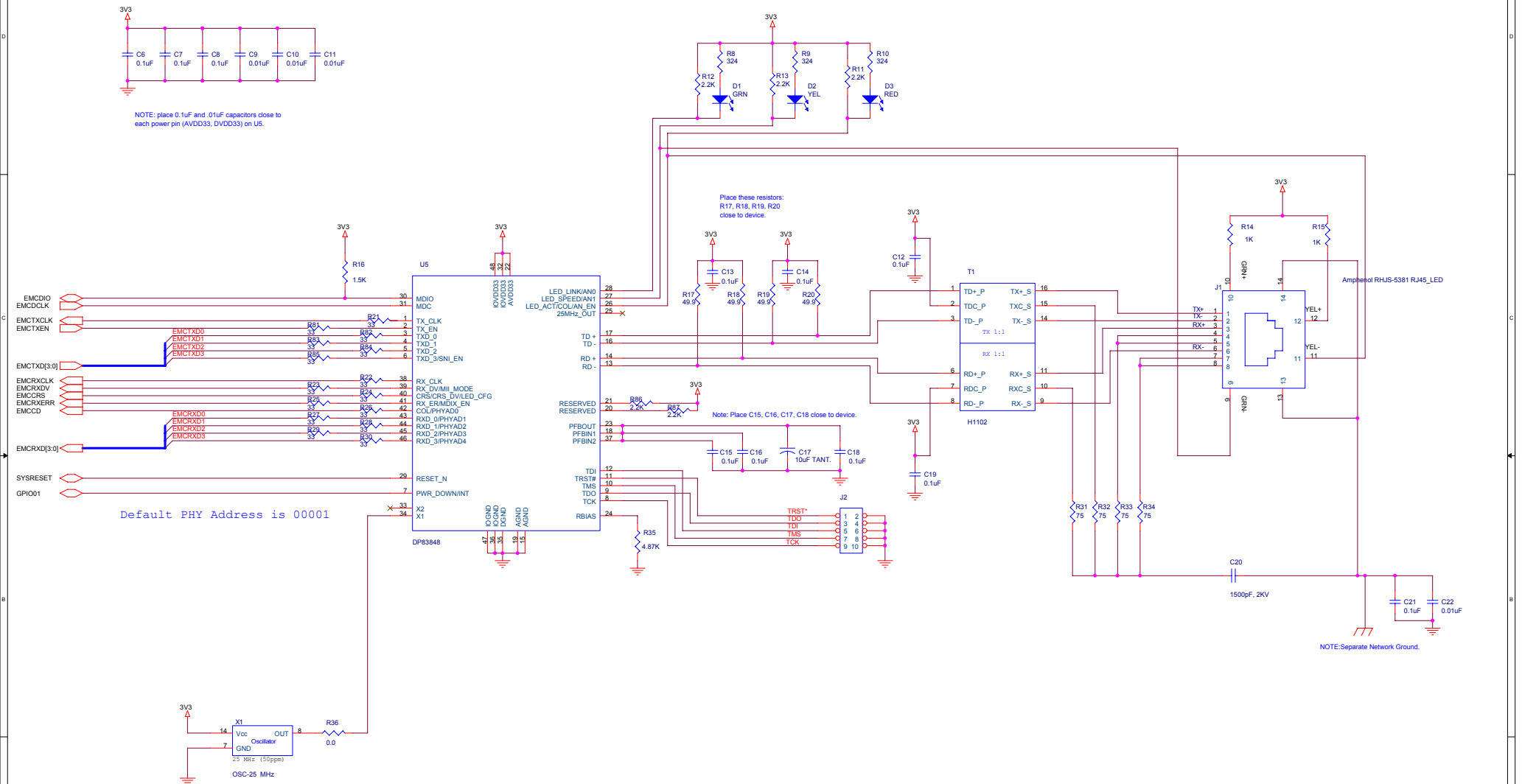
- Rev A - Initial draft.
- Rev B - Change of LEDs on DP83848.
  - Pin 28 to LED\_LINK
  - Pin 27 to LED\_SPEED
  - Pin 26 to LED\_ACT/COL
  - Connect jack's LEDs to SPEED and ACT
- Rev C
  - Change DP83848 pinouts to reflect July 04 datasheet.
- Rev D
  - Default is MII mode
  - Use Pulse H1102 as reference magnetic
  - Default is PHYAD = 1
  - AN\_EN, ANO, AN1 have internal pull-ups
  - Default is Auto-MDIX enable
- Rev E
  - Changed RBIAS resistor to 4.87K (1%)
  - Added 2.2K pull-ups to reserved pins (20, 21)
  - Changed resistor value for pull-ups and pull-downs to 2.2K
  - Added 33 ohm in series with MII signal lines
  - Updated pinouts to reflect March 05 datasheet

#### RMII Clock Operation



Note: For Reference Only

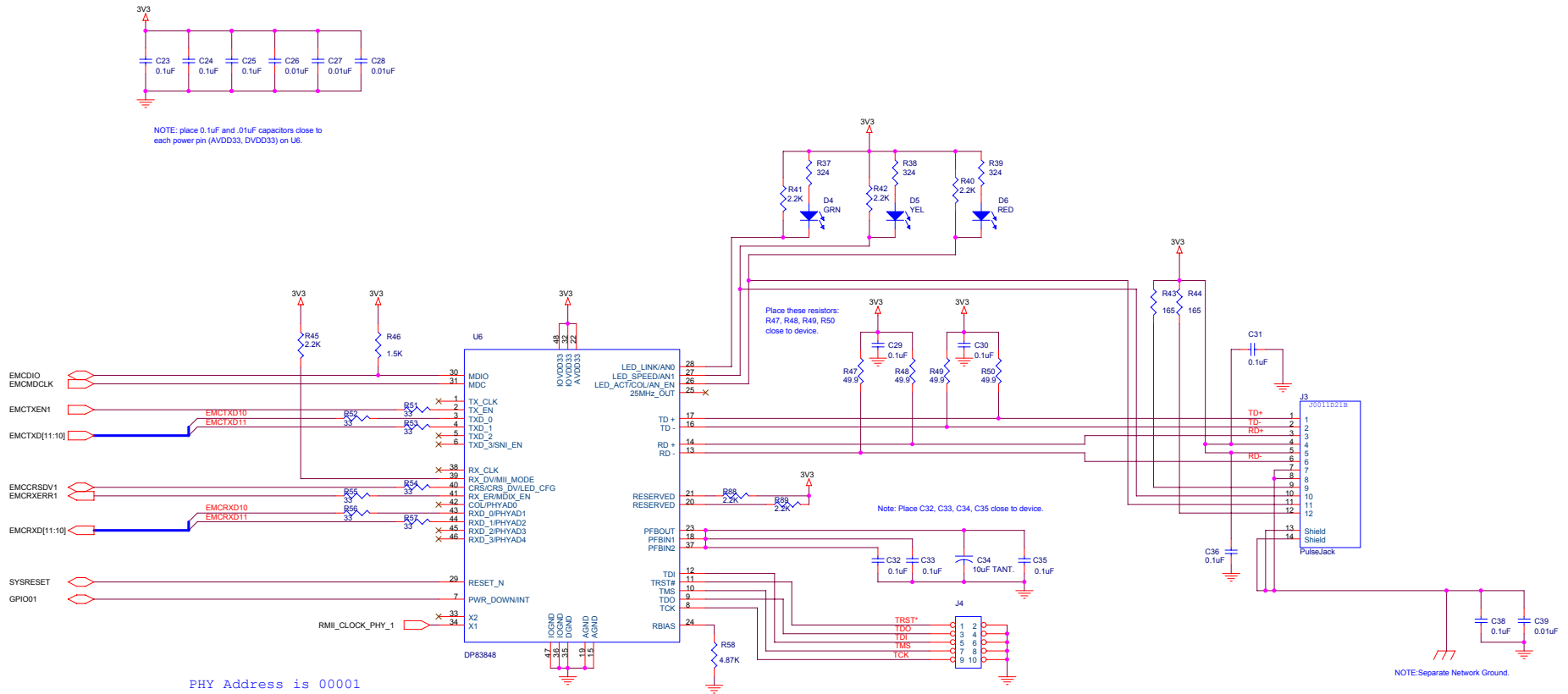
# MII ETHERNET PHY



Title		IBM PPC440G/NSC DP83848 App. Note	
Size		Document Number	
C		CID Working Draft: MII Ethernet	
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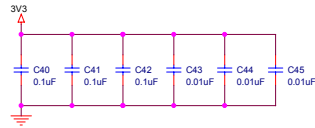
Note: For Reference Only

## RMII ETHERNET PHY 1

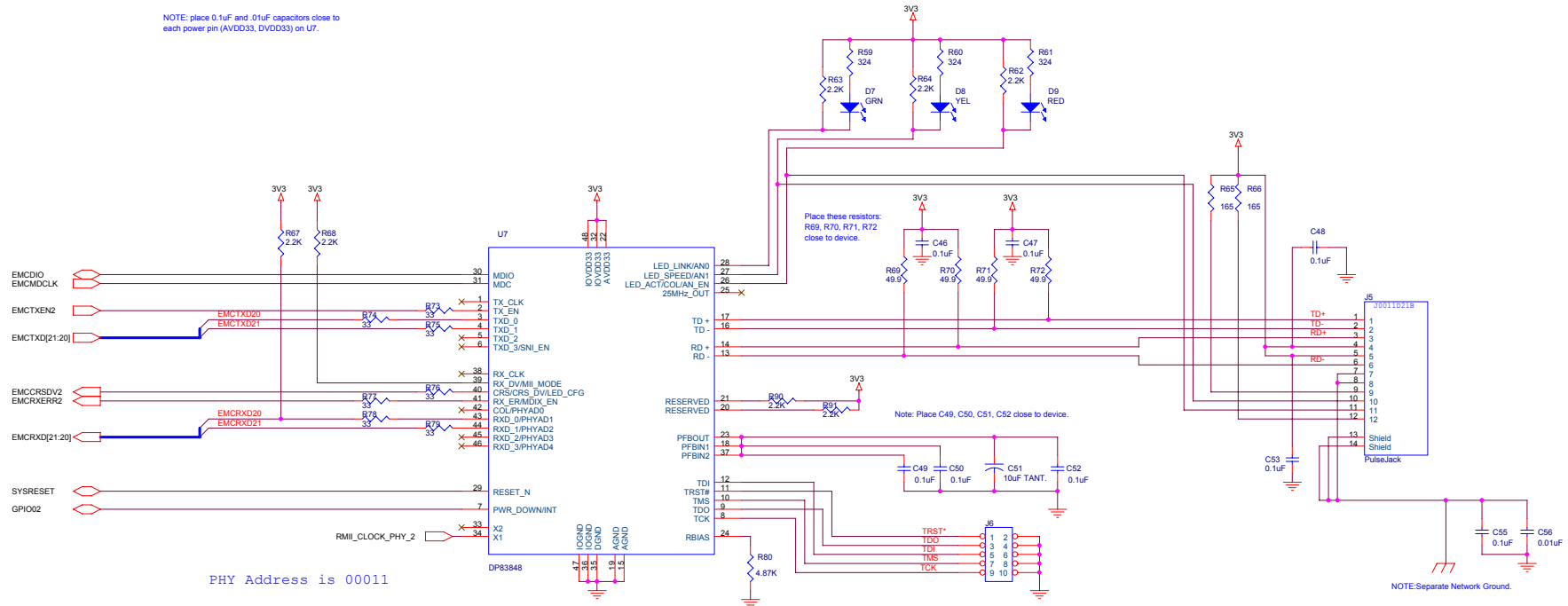


Note: For Reference Only

# RMIi ETHERNET PHY 2



NOTE: place 0.1uF and .01uF capacitors close to each power pin (AVDD33, DVDD33) on U7.



PHY Address is 00011

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